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Efficient Design of Approximate Multiplier using High-Speed Adder Compressor

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Abstract: In this modern era, many digital systems are error-resilient, which allows us to take advantage of approximate computations. It makes the use of replacement of identical computing units by their counterparts. Approximate computing can also decrease the complexity at the designing levels by increasing performance and power efficiency. Adders and multipliers are the basic buildings blocks of many digital applications. These blocks are approximated in several ways. Research works are on the rise at many levels on approximate computing. Approximation at the designing level is more advantageous as the modifications are much easier than the preceding levels. A method of designing an Approximate Multiplier (AM) with a novel structure introduced in a 16-bit adder compressor is proposed. The 16-bit Adder Compressor (AC) is designed with 8-2 adder compressors in general. The 8-2 adder compressor is designed with 7-2 and 3-2 adder compressors and half adders. The existing and proposed multiplier is designed using Xilinx 14.7 in the frontend. The speed of the proposed multiplier is a 55.44% increase compared to Existing Multiplier.

Index Terms **- 7-2 and 3-2 AC, AM, approximate computing.**

I. INTRODUCTION

The need for approximation arises from the fact that exact computation requires more energy in different applications. That means wherever the accuracy is not a significant concern, and the design has to be energy efficient, we may take advantage of approximation that requires less energy than the exact one. For most digital circuits, adders and multipliers are the basic building blocks. Replacing the same building blocks with approximate ones results in energy-efficient designs. A multiplier is a device that multiplies any two operands and gives the corresponding result. Multiplication is nothing but the repeated addition of partial products. This involves adding partial products by using half adders and full adders based on the bit size of input operands. Logic gates are used to implement these adder circuits under different technologies. In the design of high-speed multipliers, compressors are used in the reduction tree to speed up the process. These compressors are implemented using full adders.

Moreover, the Integrated circuit(IC) era of emerging digital trends prefers compact size. This ensures the necessity of area-efficient designs for most of the digital circuits. At the same time, it allows the approximate values but not the exact ones to implement energy-efficient designs. To make the most of error tolerance, various techniques are available. These are of three types: (1) insistent voltage scaling; (2) truncation of bit-width; (3) use of imprecise building blocks.

The concept in [1] is imperfect, full adder cells to implement the multi-bit adder cells with minimized complexity at the transistor level. Reflection of errors due to approximation typical digital processing at higher levels may not impact the output quality much. Two new methods for approximate 4-2 compressors are proposed in [2] for implementing a multiplier and are analyzed for a dadda multiplier. Simulation of these methods at 1GHz frequency revealed significantly reduced power, delay, and transistor count. It uses XOR-XNOR combinations for the implementation of the compressor. [3] Proposed AMs for DSP applications. This technique takes „m‟ concomitant bits (i.e., m-bit segment) from each n-bit operand where m is greater than or equal to „n/2‟. An m-bit segment can start only from one of two or three fixed bit positions depending on where the leading one bit is located for a positive number. This can provide much higher accuracy. AM circuits proposed in [4] use the technique of partial product perforation. In this technique, the errors are bound and predictable. This approach can be used for any multiplier regardless of its architecture. Perforation skips the generation of partial products instead of cutting them. Thu decreasing the number of operands to be accumulated, reducing the delay. An AM with configurable partial error recovery is proposed in [5]. This mainly focuses on mitigating critical paths by using only simple but fast adders in the reduction tree. An inaccurate 4-2 counter is used for error correction in implementing the multiplier proposed in [6]. The existing multiplier [7] proposed two multipliers, one is for approximating all columns, and the second one approximates the least significant columns. It is based on the probability statistics of the logic block results. This paper presents a new approach for AM design using 16-bit AC.

Contribution of Paper, Briefly introduction AM applications in Section 1 and corresponding AM Literature Survey is seen in section 2. Architecture Explanation of Existing and Proposed AM see in section 3 and section 4. Finally, the Results Explanation and conclusion see in sections 5 and section 6.